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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,847	02/20/2002	Kuan-Yu Lee	SUND 279	3153

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/077,847	LEE ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending for examination

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiedenman et al U.S. Patent 4,334,287 in view of So et al U.S. Patent 6,307,776.

4. As per claim 1, Wiedenman et al teach a circuit apparatus with general purpose input output pins, comprising:

a memory [128 fig. 1], which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory [inherent];

a control processing unit having a data pin [104 fig. 1], wherein the data pin is coupled to the memory pin [104-128 fig. 1]; and

a buffer [112 fig. 1], coupled to the data pin, for receiving an input signal and feeding the input signal into the control-processing unit [col. 1 lines 9-17; col. 3 lines 35-39].

Wiedenman et al teach the arrangement of the system includes a buffer memory into which data from the peripheral or I/O units may be stored or from which data may be read for application to the peripheral or I/O units. However, Wiedenman et al do not teach expressly the

buffer receiving and feeding the input signal into the control-processing unit according to a control signal synchronized with the recharging signal.

So et al teach another system which comprising an memory, which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory; and a buffer for receiving an input signal. Specifically, So et al teach a buffer [610 fig. 6] for receiving an input signal [Din] and feeding the input signal into the control processing[1] unit according to a control signal [from 645 fig. 6] synchronized with refresh operation [col. 10 lines 12-13; lines 17-21].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Wiedenman et al with the re-routing of data to a processing unit during the recharging of the memory unit as taught by So. et al.

The motivation for doing so would have been to provide a system that can operates at a faster speed so that data can be processes efficiently and without undue delays.

Therefore, it would have been obvious to combine the system of Wiedenman et al with So et al to obtain the invention as specified in claim 1.

5. As per claim 2, Wiedenman et al teach control-processing unit [col. 1 lines 15-16]. Wiedenman et al do not teach expressly the control processing unit is an Application Specific Integrated Circuit. However, It would have been obvious to one of ordinary skill in the art that the generic unit which is coupled to the memory encompasses different processing unit including

[1] A control-processing unit is not explicitly shown in the reference. However, as line 18 of col. 10 shows, if buffer contains the *data corresponding to* a *read address,* the data is route from buffer to the output. Therefore, it would have been obvious to one of ordinary skill that the output could be feeding the input signal to a processing unit.

the claimed ASIC because the special structure of the processing unit does not affect the data output switching operation of the memory and buffer.

6. As per claim 3, Wiedenman et al do not teach the claimed buffer model. It would have been obvious to one of ordinary skill in the art the generic buffer encompasses different buffers including the claimed buffer type because the special structure of the buffer does not affect the data output switching operation of the memory and buffer.

7. As per claim 4, So et al teach the memory is a DRAM [col. 4, line 42 – 46];

8. As per claim 5, Wiedenman et al teach the control signal is sent from the control-processing unit [col. 4 lines 62-65].

9. As per claim 6, Wiedenman et al teach a circuit apparatus with general purpose input output pins, comprising:

a memory [128 fig. 1], which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory [inherent];

a control processing unit having a data pin [104 fig. 1], wherein the data pin is coupled to the memory pin [104-128 fig. 1]; and

a buffer [112 fig. 1], coupled to the data pin, for receiving an input signal and feeding the input signal into the control-processing unit [col. 1 lines 9-17; col. 3 lines 35-39].

Wiedenman et al teach the arrangement of the system includes a buffer memory into which data from the peripheral or I/O units may be stored or from which data may be read for

application to the peripheral or I/O units. However, Wiedenman et al do not teach expressly the buffer for output an output signal from the control processing unit, wherein the buffer outputs the output signal according to a control signal synchronized with the recharging signal.

So et al teach another system which comprising an memory, which has a memory pin and is refreshed by a recharging signal to maintain stored data in the memory; and a buffer for receiving an input signal. Specifically, So et al teach a buffer [610] for outputting an output signal from the control processing unit [Din is an input signal from the control processor and routed to Data output 660 fig. 6], wherein the buffer outputs the output signal according to a control signal synchronized with the recharging signal [col. 10 lines 17-21].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of Wiedenman et al with the re-routing of data to a output during the recharging of the memory unit as taught by So. et al.

The motivation for doing so would have been to provide a system that can operates at a faster speed so that data can be processes efficiently and without undue delays.

Therefore, it would have been obvious to combine the system of Wiedenman et al with So et al to obtain the invention as specified in claim 6.

10. As per claim 7, see discussion in claim 2.

11. As per claim 8, see discussion in claim 3.

12. As per claim 9, see discussion in claim 4.

13. As per claim 10, see discussion in claim 5.

14. Claims 1, 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Keeth et al U.S. Patent 6,445,636.

Keeth et al discloses a circuit apparatus with General Purpose Input Output (GPIO) pins comprising:

a memory [12 a fig. 3], which has a memory pin [inherent] and is refreshed by a recharging signal to maintain stored data in the memory [col. 5 lines 13-15];

a control processing unit [202 fig. 5] having a data pin [inherent], wherein the data pin is coupled to the memory pin [236 fig. 5]; and

a secondary memory [12 b fig. 3 – located in the cache memory 236 fig. 3], couple to the data pin [col. 7 lines 12-22], for receiving an input signal and feeding the input signal into the control processing unit [from col. 5 line 64 to col. 6 line 1; lines 41-56] according to a control signal synchronized with the recharging signal [col. 3 lines 45-53; col. 6 lines 22-27]

Keeth et al do not disclose expressly the secondary memory as a buffer.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the secondary memory of Keeth et al with a buffer because applicant has not disclosed that the claim buffer provides an advantage over the memory teach by Keeth et al. One of ordinary skill in the art, further more, would have expected applicant's invention to perform equally well with the secondary memory because it allows the processor the abilities to write or read data without undue delay.

Therefore, it would have been an obvious matter of design choice to modify the secondary of Keeth et al system to obtain the invention as specified in claim 1 and 6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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